What is claimed is:

1. A layout method of a semiconductor device comprising the steps of:

arranging active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between the more than one first and second electrodes of those active regions by positioning at least two or more gates having predetermined width and length at a substantially constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

2. The method, as defined in claim 1, wherein the length of the dummy gates is the same as that of the gates of the transistors.

3. The method, as defined in claim 1, wherein at least more than one gate of the plurality of transistors have common terminals each of which is commonly connected on the substrate of the semiconductor device.

4. The method, as defined in claim 1, wherein a plurality of dummy gates are commonly connected on the substrate.

5. A layout method of sense amplifier of a semiconductor device, wherein the sense amplifier amplifies and outputs the difference between the first and second input data applied by data input transistors and more than one control signal input transistors to which the control signals are applied, the method comprising the steps of:

arranging active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning two or more gates having predetermined width and length at a substantially constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between the data and control signal input transistors at substantially the same gap as that of the gates divided from the data and control signal input transistors on the substrate.

6. The method, as defined in claim 5, wherein the dummy gates have a predetermined width, that is, the same as that of the gates which are largest in width among those divided gates of a plurality of transistors.

7. The method, as defined in claim 5, wherein the length of the dummy gates is substantially the same as that of the gates.

8. The method, as defined in claim 5, wherein at least more than one gate of the data and control signal input transistors have common terminals each of which is commonly connected on the substrate.

9. The method, as defined in claim 5, wherein a plurality of dummy gates are commonly connected on the substrate.

10. A layout method of a semiconductor device comprising the steps of:

arranging active regions of a plurality of transistors having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning at least more than one gates having predetermined width and length at a substantially constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between and outside a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

11. The method, as defined in claim 10, wherein the length of the gates of the transistors is substantially the same as that of the dummy gates.

12. The method, as defined in claim 10, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate of the semiconductor device.

13. The method, as defined in claim 10, wherein a plurality of dummy gates are commonly connected on the substrate.

14. A semiconductor device comprising:

a substrate;

active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes on the substrate;

a plurality of gates of transistors disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more gates are of a predetermined width and length at a substantially constant gap on the substrate; and

a plurality of dummy gates having predetermined width and length between a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

15. The device, as defined in claim 14, wherein the length of the dummy gates is substantially the same as that of the gates of the transistors.

16. The device, as defined in claim 14, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

17. The device, as defined in claim 14, wherein a plurality of dummy gates are commonly connected on the substrate.

18. A semiconductor device comprising:

a substrate;

active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of gates of transistors disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate is of predetermined width and length at a substantially constant gap on the substrate; and

a plurality of dummy gates having predetermined width and length between and outside a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

19. The device, as defined in claim 18, wherein the length of the dummy gates is substantially the same as that of the gates of the transistors.

20. The device, as defined in claim 18 wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

21. The device, as defined in claim 18, wherein a plurality of dummy gates are commonly connected on the substrate.

22. A semiconductor device comprising:

a substrate;

active regions of a plurality of transistors having at least more than one first and second electrodes disposed on the substrate;

a plurality of gates of transistors between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate has a predetermined width and length at a substantially constant gap on the substrate; and

a plurality of dummy gates having predetermined width and length outside a plurality of transistors at substantially the same gap as that of the transistor gates on the substrate.

23. The device, as defined in claim 22, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

24. The device, as defined in claim 22, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

25. The device, as defined in claim 22, wherein a plurality of dummy gates are commonly connected on the substrate.

26. A semiconductor device comprising:

a substrate;

active regions of transistor, the active regions having at least one first and second electrodes on the substrate;

at least one gate layer disposed on the active regions between the first and second electrode, wherein the gate electrode layer is a predetermined width and length; and

a plurality of dummy gate layers disposed between and outside of the active region and having predetermined width and length at a substantially constant gap from the gate layer.

27. The device, as defined in claim 26, wherein the lengths of the dummy gates layers are substantially the same as that of the gate electrode layer of the transistor.

28. The device, as defined in claim 26, wherein the plurality of dummy gates layers are commonly connected on the substrate.